

A Decentralized Scalable Control Architecture for Islanded Operation of Parallel DC/AC Inverters with Prescribed Power Sharing

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Abstract—This paper addresses the problem of output voltage regulation at the point of common coupling (PCC) for multiple single-phase DC/AC inverters connected to a microgrid in islanded mode, and prescribes a robust *decentralized* scheme for sharing power among different sources. The problem of regulating voltage at PCC is posed as a disturbance-rejection problem, where the load current is regarded as an *unknown* disturbance signal and thus no assumptions are made regarding the power demanded by the load at the PCC. The disturbance-rejection controller has an inner-outer cascaded structure, where inner-current controller is parameterized by coupling inductance of the inverter, and is such that the inner-loop seen by the outer-voltage controller is identical for all the parallel inverters. This favors *scalability* by allowing multiple inverters to be added to the PCC without the need to separately design outer-loop controllers for individual inverters. A significant feature of the proposed control architecture is that the stability and performance analysis of the multi-inverter network is tractable; in fact, analysis can be done in terms of an equivalent *single-inverter* system. Case studies presented in this paper demonstrate the effectiveness of the proposed design in terms of voltage regulation, power sharing and robustness to parametric and modeling uncertainties.

I. INTRODUCTION

The liberalization of the present electricity market and the flexibility offered by power electronic devices have resulted in significant interest in the concept of microgrids. Microgrids [1] are localized grid systems that allow integration of local power sources, such as photovoltaics (PVs), wind, battery and other distributed energy resources (DERs) with local loads connected at the PCC. Fig. 1 represents a schematic of a microgrid. In such microgrids, multiple DC power sources connected in parallel, each interfaced with DC/DC converter, provide power at their common output, the DC-link, at a desired regulated voltage. These DC-links in turn are connected to an AC load at the PCC through a parallel operation of the voltage-source DC/AC inverters. Such parallelization enables higher output power, reliability and ease of use.

Microgrids can be operated in both grid-tied or islanded mode. The two modes of operation pose different requirements on the control design for parallel operation of the voltage-source inverters (VSIs). Note that the islanded operation is particularly challenging since it requires regulating the desired voltage and frequency at the PCC. Two main control architectures are employed for islanded operation of

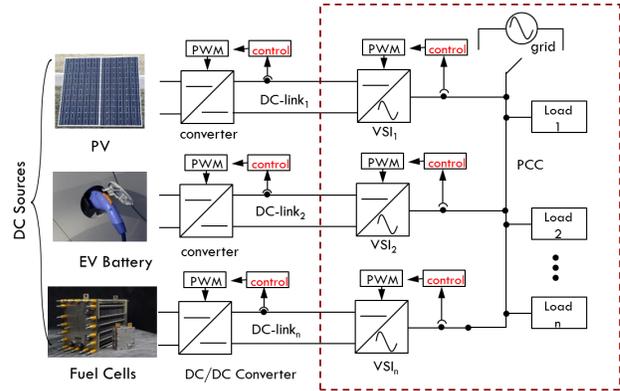


Fig. 1: A schematic of a microgrid. An array of DC power sources provide power at the respective DC-links, where the voltage is regulated by DC/DC converters. A network of parallel inverters that connect to the DC-links convert the total current from the sources at the regulated voltage to alternating current (AC) at its output to satisfy the power demands of the AC loads.

microgrids [2] - (a) *Single master operation*: In this setup, a single *master* inverter acts as a VSI and is used for regulating reference voltage and frequency at the PCC, while other inverters are required to supply specified active and reactive power set-points (similar to grid-tied mode of operation). Such a scheme has a single point of failure and is non-robust to failure of the master VSI. (b) *Multi master operation*: In this mode of operation, several inverters act as VSIs with pre-defined frequency/active power and voltage/reactive power characteristics. This architecture avoids single point of failure; however at the cost of increased complexity of the control design. The architecture proposed in this article is based on multi master mode of operation.

Apart from maintaining voltage and frequency stabilities at the PCC, another important task for islanded operation of microgrids is to share the load demand among multiple parallel connected VSIs in the prescribed proportions, which may be dictated by the individual power ratings of the VSIs or external economic criteria [3]. The main challenges arise from the uncertainties in the size and the schedules of loads, the complexity of a coupled multi-inverter network, and the uncertainties in the model parameters at each inverter. Droop-based strategies [4] that mimic control architecture for traditional grids have extensively been used and provide significant flexibility in terms of plug and play capabilities of the distributed generation (DG) units and higher reliability in terms of decentralized implementation (no communication lines); However droop-based control inherits undesirable trade-off between voltage regulation and load sharing. More

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The authors would like to acknowledge ARPA-E NODES program for supporting this work.

importantly, droop-based strategies result in slow dynamic response of the microgrid system and are dependent on line impedance (i.e., $Q - V$ and $P - \theta$ droop control strategy is used in inductive line and $Q - \theta$ and $P - V$ droop control strategy is used in resistive lines). Moreover, the droop method results in system instability when the slope of the droop characteristics is small [5], [6].

While there is substantial literature on detailed modeling of VSIs for inverter-level analysis, the literature on stability and performance analysis at the distribution system level is impractical. The major difficulty for analyzing droop-controlled VSIs arise from the availability of only *local* measurements [7]. Another challenge in the control design for a microgrid is that the power demanded by load at the PCC is uncertain and time-varying. Typical methods in the existing literature address the problem of voltage (and frequency) regulation in presence of *unknown* loads either by using adaptive control [8] (which often requires knowledge of nominal load power), or by letting the voltage and frequency droop in a controlled manner (which inherits the problems of droop-based designs described above).

In this paper, we propose a scalable control framework to address all the above concerns for islanded operation of parallel VSIs. The controllers are obtained systematically using an *inner-outer* structure, where the inner-current controller accounts for regulating the output current of VSI to the desired reference and is suited for grid-tied mode of operation of microgrids. The outer-controller in turn is designed to regulate the output voltage (and frequency) at the PCC. The controllers are obtained using loop-shaping technique [9], where the performance specifications are encoded directly into control synthesis. These specifications also include sufficient gain and phase margins for the closed-loop system to ensure robustness to modeling and parametric uncertainties. Moreover, the choice of low-order controllers provide practical feasibility in terms of implementation.

Furthermore, we build upon the power sharing controller for DC/DC converters in our prior work [10] and extend the sharing architecture to a network of parallel VSIs for *isochronous* operation (i.e., existence of common time reference among inverters) to overcome the limitations of droop-based control strategies, while still retaining the advantages of droop-based designs. In particular, we focus on *multi master* mode of operation and propose a sharing strategy that makes the stability and performance analysis viable for the parallel inverter system. In fact it is shown later that performance and stability of the proposed coupled multi-inverters network is analyzed by considering an *equivalent* single VSI system.

Additionally, the voltage (and frequency) regulation is cast a *disturbance-rejection* problem, where the load current is treated as an external disturbance signal. This viewpoint enables robustness to deviations from nominal loading conditions. Furthermore, this viewpoint allows to incorporate non-linear loads into the network without the need to measure the load current separately. Thus the proposed method facilitates for *decentralized* implementation and does not require separate communication lines for sharing common measurement

information.

II. AVERAGED MODELING OF FULL-BRIDGE INVERTERS

In this section, we describe dynamic models of full-bridge DC/AC inverters, which transform a source of direct current (DC) to an equivalent source of alternating current (AC) using semiconductor switches. The model presented below depicts dynamics for signals that are averaged over a switch cycle.

Fig. 2a shows the schematic of a full-bridge inverter. A full-bridge inverter [11] comprises of two legs each containing two switches - (a) s_1 and s_2 , (b) s_3 and s_4 . The full-bridge inverter is interfaced with the AC-side load through an interface reactor represented by a series RL branch. L and R respectively, represent the inductance and internal resistance of the interface reactor. The interface reactor acts as a low pass filter and ensures low-ripple AC-side current i_L resulting from switching operations. The voltage at terminal a is controlled by periodically switching ON/OFF the switches s_1 and s_2 . Similarly, switches s_3 and s_4 control the voltage at terminal b . The quantities $V(t)$ and $i_{load}(t)$ represent the AC-side voltage (or output voltage), and load current, respectively. Let $d_a(t)$ represent the proportion of ON time of switch s_1 (or OFF time of switch s_2), also known as the *duty-cycle* of switch s_1 . Therefore the average voltage at terminal a , $V_a(t)$ is given by $V_a(t) = d_a(t)V_{dc}$, where V_{dc} is the voltage of the DC source. Similarly, the voltage V_b at terminal b , averaged over switching cycles, is given by $V_b(t) = d_b(t)V_{dc}$. By combining the two states of operation, dynamic model of a full-bridge inverter (averaged over switching cycles) is given as

$$\begin{aligned} L \frac{di_L(t)}{dt} + Ri_L(t) &= \underbrace{(d_a(t) - d_b(t)) V_{dc} - V(t)}_{u(t) := m(t)V_{dc} - V(t)} \\ C \frac{dV(t)}{dt} &= i_L(t) - i_{load}(t). \end{aligned} \quad (1)$$

The average voltage between terminals a and b , $\tilde{u}(t) := m(t)V_{dc}$ is proportional to, and can be controlled by the modulating signal $m(t) \in [-1, 1]$. Fig. 2b shows a control block diagram of the system described by Eq. (1), for which the next section presents a closed-loop control structure to regulate $V(t)$ at its reference value. Note that for a given value of modulating signal $m(t) := d_a(t) - d_b(t)$, there are infinitely many choices for the duty-cycles $d_a(t)$ and $d_b(t)$. This issue of non-uniqueness is addressed by considering the following scheme:

$$\begin{array}{c} d_a(t) \\ d_b(t) \end{array} \begin{array}{|c|c|} \hline m(t) \geq 0 & m(t) < 0 \\ \hline m(t) & 0 \\ \hline 0 & -m(t) \\ \hline \end{array}$$

Remark: An important contribution of this paper is that it introduces a control architecture for a paralleled network of inverters for which performance analysis becomes feasible. The proposed architecture is scalable and extends to any number of inverters in the network. In fact it is later shown that the performance analysis of the networked system is

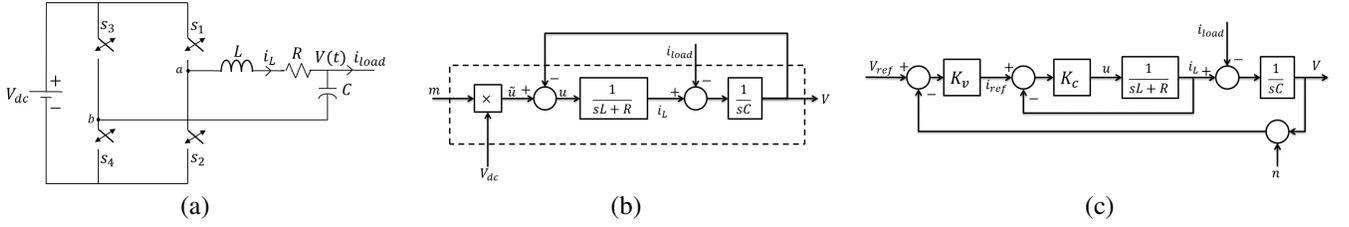


Fig. 2: (a) Circuit representing a full-bridge inverter. The AC-side current is given by i_{load} . The switches s_1, s_2, s_3 and s_4 control the AC-side voltage $V(t)$. (b) Associated control model of the full-bridge inverter. (c) Inner-outer control architecture of a full-bridge inverter.

identical to the performance analysis of an *equivalent* single-inverter system. The following section discusses the control design scheme of a single-inverter system. A simple lead-lag based inner-outer controller is employed for voltage regulation. Readers familiar with lead-lag based designs may skip this section without losing the thrust of the paper.

III. CONTROL OF SINGLE INVERTER

Any controller that is required to regulate the output voltage $V(t)$ at its reference value, must do so through an equivalent control of the modulating signal $m(t)$. However for the purpose of control design and implementation, one must focus directly on the control input $u(t)$, which in turn determines the modulating signal $m(t) = (u(t) + V(t))/V_{dc}$.

The objective of voltage regulation is achieved using a nested inner-current outer-voltage control architecture, shown in Fig. 2c. The outer-voltage controller K_v generates a current reference i_{ref} for the inner-loop. The inner-current controller K_c regulates the inductor current i_L to the desired i_{ref} . The quantity V_{ref} represents the desired reference voltage signal. For the purpose of control design, it is assumed that the signals $i_L(t)$ and $V(t)$ are available for measurements. The total current drawn at the PCC, which comprises of load current and any unmodeled disturbances, is denoted by i_{load} . For simplicity, we use $G_c := \frac{1}{sL + R}$ and $G_v := \frac{1}{sC}$ to denote the plant transfer functions in the inner and outer loops.

A. Design of Inner-loop Controller

In our architecture, the main objective of the inner-controller K_c is to ensure regulation of inductor current i_L to the reference i_{ref} generated by K_v . Since the AC signal pulsates at $\omega_n = 60\text{Hz}$, K_c must ensure robust tracking at frequencies at least till ω_n . Additionally, it is preferred to have a relatively low-order controller K_c . These objectives are achieved through an appropriate *loop shaping* using a lead-lag controller as described below. Readers conversant with the concept of loopshaping may skip the following discussion and directly refer to (4) and (5) for inner-loop controller parameterization.

Let us assume that i_{ref} is required to be tracked with a *closed-loop* bandwidth of $\omega_b (\sim 10\omega_n)$; ω_b is chosen sufficiently large such that the inner closed-loop system from i_{ref} to i_L has unity gain till ω_n with zero-phase delay, and is small enough to ensure that the switching ripple content of the control signal u is low. In the loop shaping procedure, the desired performance objectives are specified

in terms of the properties of the loop transfer function $l(s) = G_c(s)K_c(s)$. For achieving zero steady-state error at ω_n , the controller must be equipped with a pair of complex-conjugate poles at $s = \pm j\omega_n$, also referred as resonant controller in the literature [12]. Furthermore the open-loop plant $G_c(s)$ contains a pole at $s = -R/L$, which in turn introduces a -90° phase delay for frequencies larger than $10R/L$. Therefore, to improve the loop-gain phase, a zero at $s = -R/L$ is introduced. This pole-zero cancellation is admissible since the pole is on the left half plane (LHP). Thus the modified inner-loop controller assumes the form,

$$K_c(s) = \left(\frac{sL + R}{s^2 + \omega_n^2} \right) H(s). \quad (2)$$

Note that the resonant controller $1/(s^2 + \omega_n^2)$ introduces a -180° phase delay at and beyond ω_n . However to achieve a stable closed-loop system, the loop-gain phase at the gain crossover frequency $\omega_c \approx \omega_b/1.5$ must be larger than -180° by a value that is referred to as the phase-margin. For robust stability, a phase-margin of about 60° is required, which can be achieved by using a lead filter of the form $F_{lead}(s) = \left(\frac{s + \omega_c/\sqrt{\alpha}}{s + \omega_c\sqrt{\alpha}} \right)$, where $\alpha = 13.93$. For achieving zero steady-state error at DC, the magnitude of loop-gain must be large ($\sim 50\text{dB}$) at low frequencies, i.e. $|l(j0)| = 10^{2.5}$. The loop-gain magnitude is increased at low frequencies using a lag-filter, $F_{lag}(s) = \left(\frac{s + \beta}{s + \delta\beta} \right)$, where $\beta \sim 2 \text{ rad/s}$ and $\delta < 1, \delta \in \mathbb{R}_+$. Note that F_{lag} has the property that $F_{lag}(j\omega) \approx 1$ for frequencies larger than about 20 rad/s. Therefore, it does not change the phase or magnitude of the loop-gain around the crossover frequency ω_c . Thus the transfer function $H(s)$ in Eq. (2) is expressed as

$$H(s) = h \underbrace{\left(\frac{s + \beta}{s + \delta\beta} \right)}_{F_{lag}(s)} \underbrace{\left(\frac{s + \omega_c/\sqrt{\alpha}}{s + \omega_c\sqrt{\alpha}} \right)}_{F_{lead}(s)}, \quad (3)$$

where $h \in \mathbb{R}$ ensures that $|l(j\omega_c)| = 1$. Therefore, the inner-loop controller K_c assumes the following modified form

$$K_c(s) = h \left(\frac{sL + R}{s^2 + \omega_n^2} \right) \left(\frac{s + \beta}{s + \delta\beta} \right) \left(\frac{s + \omega_c/\sqrt{\alpha}}{s + \omega_c\sqrt{\alpha}} \right), \quad (4)$$

where h and δ satisfy the following equations

$$h = \sqrt{\alpha} (\omega_c^2 - \omega_n^2) \quad \text{and} \quad \delta = \frac{h}{10^{2.5}\alpha\omega_n^2}. \quad (5)$$

Remark: In the grid-tied mode, an inverter is just controlled to be a current source and does not require an outer-voltage loop, since the PCC voltage is fixed by the utility grid.

B. Design of Outer-loop Controller

The inner-loop controller K_c ensures that the inductor current tracks the current reference i_{ref} . However, i_{ref} is an internal signal in the closed-loop system of Fig. 2c and is produced by the outer-voltage controller K_v which is designed to regulate the AC-side voltage V at its reference value V_{ref} . Since the objectives of the outer-loop are similar to those of the inner-loop (albeit in terms of the voltage signal), we use the design methodology as proposed in previous Sec. III-A.

Note that the outer-loop plant $G_v(s) = 1/sC$ introduces large gains in the loop-transfer function $\tilde{l}(s) = G_v(s)K_v(s)$ at low-frequencies. Thus a lag-controller is not required for the outer-loop control design. In an inner-outer cascaded control design, the outer-loop controller is the primary controller that regulates the primary controlled variable (V) at the desired reference, whereas the inner-loop (secondary) controller rejects any input disturbance locally before it propagates to the outer-loop plant (G_v). Thus for a cascaded design to function properly, the inner-loop must respond much faster than the outer-loop. This is achieved by ascribing the outer-loop controller K_v such that the outer loop-gain crossover frequency $\tilde{\omega}_c \sim 0.4 - 0.5\omega_c$. Thus $K_v(s)$ assumes the following functional form

$$K_v(s) = \tilde{h}C \left(\frac{s + \beta}{s^2 + \omega_n^2} \right) \left(\frac{s + \tilde{\omega}_c/\sqrt{\alpha}}{s + \tilde{\omega}_c\sqrt{\alpha}} \right), \quad (6)$$

where $\tilde{h} \in \mathbb{R}$ is chosen such that $|\tilde{l}(j\tilde{\omega}_c)| = 1$ and is given by

$$\tilde{h} = \tilde{\omega}_c \sqrt{\frac{\alpha}{\beta^2 + \tilde{\omega}_c^2}} (\tilde{\omega}_c^2 - \omega_n^2). \quad (7)$$

Remark: The inner-loop controller K_c depends on the inverter parameters L and R , while the outer-loop controller K_v depends on the capacitance C at the output. This parametric dependence (and inner-outer decoupling) is exploited in the next section to extend the control design to multiple parallel inverter system.

IV. EXTENSION TO MULTIPLE INVERTERS CASE

A microgrid facilitates integration of multiple parallel full-bridge VSIs at the PCC. In this section, we describe a novel non-droop based decentralized power sharing scheme through an extension of the proposed single inverter control. Such an extension achieves the objective of power sharing and voltage regulation in the context of DC/DC converters too and is reported in our prior work [10]. An *isochronous* operation is assumed for the parallel inverters case, i.e., we assume existence of common time reference among inverters. This assumption is needed to ensure that all the inverters have access to the same time-domain voltage reference signal V_{ref} . Fig. 3 shows the proposed decentralized control framework for a system of m parallel inverters connected at the PCC through an output capacitor C . Since the multi-inverter system is highly coupled with individual controllers having access only to *local* current measurements i_{L_k} , any arbitrary choice of controller transfer functions

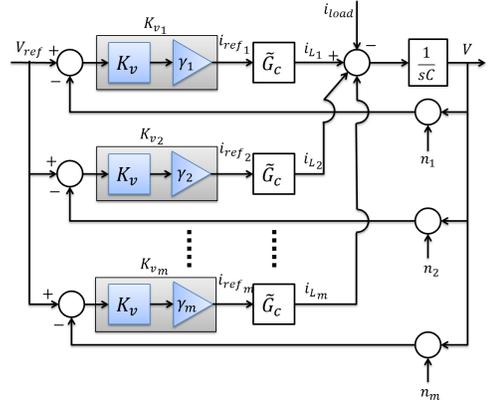


Fig. 3: Proposed decentralized framework with *smart* choices of controller parameters. The inner-current controllers K_{c_k} are chosen such that the inner-shaped plant mimics $\tilde{G}_c(s)$ shown in the discussion after Eq. (8). The outer-loop controllers are scalar multiples of the nominal outer-loop controller K_v ; the scalars γ_k govern the power-sharing requirements in a microgrid setup.

$\{K_{v_k}, K_{c_k}\}_{k=1}^m$ renders the stability and performance analysis of the multi-inverter system intractable. However, the decentralized framework is easily simplified by a *smart* choice of inner-outer controllers. For given desired gain-crossover frequencies ω_c and $\tilde{\omega}_c$ for the inner and outer-loops, respectively, we make the following two important observations -

1) The inner-controllers $K_{c_k}, k \in \{1, \dots, m\}$ are parameterized by the corresponding coupling impedances (see Eq. (4)), and therefore the respective loop-gains $l_k(s) = \frac{1}{(sL_k + R_k)} K_{c_k}(s)$ are independent of the parameters L_k and R_k as a consequence of admissible pole-zero cancellations, i.e.,

$$l_k(s) = \left(\frac{h}{s^2 + \omega_n^2} \right) \left(\frac{s + \beta}{s + \delta\beta} \right) \left(\frac{s + \omega_c/\sqrt{\alpha}}{s + \omega_c\sqrt{\alpha}} \right), \forall k. \quad (8)$$

Thus $l_1(s) = \dots = l_m(s) =: l(s)$ and therefore the closed inner-loops $\tilde{G}_{c_k} = l_k(s)/(1 + l_k(s))$ are identical, i.e., $\tilde{G}_{c_1}(s) = \dots = \tilde{G}_{c_m}(s) =: \tilde{G}_c(s)$.

2) The objective of voltage regulation at the PCC is common to all the inverters. Thus in the proposed decentralized architecture, we impose *similar* structure for the outer-voltage controllers $K_{v_k}, k \in \{1, \dots, m\}$, i.e.,

$$K_{v_k}(s) = \gamma_k \underbrace{\tilde{h}C \left(\frac{s + \beta}{s^2 + \omega_n^2} \right) \left(\frac{s + \tilde{\omega}_c/\sqrt{\alpha}}{s + \tilde{\omega}_c\sqrt{\alpha}} \right)}_{:=K_v(s)}, \forall k, \quad (9)$$

where $\gamma_k \in \mathbb{R}, \gamma_k \in [0, 1] \quad \forall k \in \{1, \dots, m\}$ and satisfy $\sum_{k=1}^m \gamma_k = 1$. The parameters γ_k are chosen to apportion power among parallel sources. We make these design specifications more precise and bring out the equivalence of the control design for the single and multiple parallel VSIs in the following theorem.

Theorem 1: Consider a single VSI system described in Fig. 2c with parameters L, R and C , and controllers K_c and K_v described by Eqs. (4) and (6), respectively; and a parallel inverter system in Fig. 3 with same output capacitance C , but

distinct inverter system parameters $\{L_k, R_k\}_{k=1}^m$ with inner and outer controllers K_{c_k} and $K_{v_k} = \gamma_k K_v$ as described in Eqs. (8) and (9) such that $\sum_{k=1}^m \gamma_k = 1$.

1. [Performance Equivalence]: The controllers K_{v_k} and K_{c_k} yield identical (to single VSI control) performance for a network of multiple parallel inverters connected at the PCC; more precisely, for the exogenous inputs - the reference V_{ref} , the load disturbance current i_{load} , and measurement-noise $n = \sum_{k=1}^m \gamma_k n_k$, the steady-state regulated signals $(V_{\text{ref}} - V, i_L, V)$ for the single-inverter system are same as the regulated signals $(V_{\text{ref}} - V, \sum_{k=1}^m i_{L_k}, V)$ for the multi-inverter system.

2. [Power Sharing]: The steady-state output currents at the PCC get divided in the ratio $\gamma_1 : \dots : \gamma_m$ up to the measurement noises; more precisely, if the measurement noise is bounded above, i.e., $(|n_k(j\omega)| < \epsilon(\omega)), \forall k$ then,

$$\left| \frac{i_{L_j}(j\omega)}{\gamma_j} - \frac{i_{L_k}(j\omega)}{\gamma_k} \right| \leq |\tilde{G}_c(j\omega)| \cdot |K_v(j\omega)| \epsilon(\omega).$$

Consequently, if $\epsilon(\omega) = 0$, then the above condition reduces to $|i_{L_1}(j\omega)| : \dots : |i_{L_m}(j\omega)| = \gamma_1 : \dots : \gamma_m$ for all ω . Thus in case of *perfect* measurements, the proportions γ_k capture the power-sharing requirements exactly.

Remark: By design, the inner-closed loop plant $\tilde{G}_c(j\omega)$ has unity gain till bandwidth and rolls-off at higher frequencies. Similarly the outer controller $K_v(j\omega)$, given by (6), rolls-off at higher frequencies. Thus the effect of high-frequency noise is mitigated by the choice of control design and the output current is apportioned according to the prescribed sharing requirements.

Proof: See appendix.

V. CASE STUDIES

In this section, we report simulation case studies to demonstrate the effectiveness of the proposed design for power sharing and voltage regulation. All simulations are done using Simulink/Simscape components, which incorporate dynamical models of batteries and generic DC sources. The customized converter/source library is available for download at [13].

A. Voltage regulation in presence of parametric uncertainties

The inner-outer controllers in Eqs. (4) and (6) are designed with high phase-margins (60°) which imparts robustness to modeling and parametric uncertainties. The simulation parameters are given below:

$$V_{\text{ref}} = A \sin(2\pi\omega_n t), \quad \text{where, } A = \begin{cases} 400V & \text{if } t < 0.2s; \\ 500V & \text{if } t \geq 0.2s. \end{cases}$$

AC-load unknown to controller,

$$(R_l, L_l) = \begin{cases} (83m\Omega, 137\mu H) & \text{if } t < 0.4s; \\ (41.5m\Omega, 68.5\mu H) & \text{if } t \geq 0.4s. \end{cases}$$

Nominal parameters : $L = 100\mu H, R = 0.88m\Omega, C = 2500\mu F$.

The controllers are designed with the nominal parametric values, while the simulations are performed with 20% uncertainty in L and C values. The desired inner-loop bandwidth

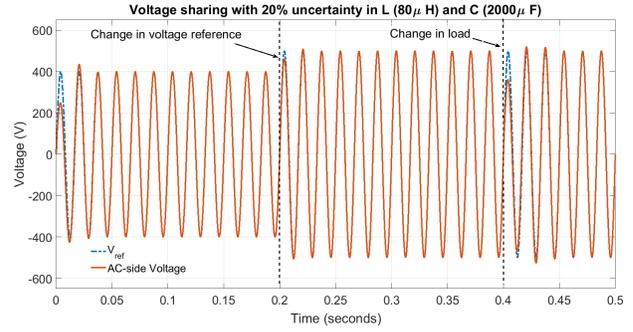


Fig. 4: Voltage regulation using the proposed controllers for 20% uncertainty in L and C values.

is chosen to be $\omega_b = 11, 100$ rad/s. The resulting inner-outer controllers are

$$K_c = \frac{20384(s + 1983)(s + 16.3)(s + 2)}{(s + 2.76e4)(s + 0.65)(s^2 + (377)^2)}$$

$$K_v = \frac{80421(s + 793.1)(s + 2)}{(s + 1.105e4)(s^2 + (377)^2)}.$$

Fig. 4 shows the result of voltage regulation for 20% uncertainty in L and C . The voltage at the PCC gets regulated at its reference V_{ref} within one cycle.

B. Power sharing among three inverters

We now substantiate the proposed non-droop based sharing for a three-inverter system. We consider three heterogeneous power sources - 1) Lithium-ion battery (Nominal voltage: 1500V, Initial State-Of-Charge: 120%), 2) Generic Source-1 (DC Voltage: 1500V), 3) Generic Source-2 (DC Voltage: 1200V). The other simulation parameters are chosen as before. The power sharing requirements are

$$\gamma_1 : \gamma_2 : \gamma_3 = \begin{cases} 0.33 : 0.33 : 0.33 & \text{if } t < 0.3s; \\ 0.70 : 0.20 : 0.10 & \text{if } t \geq 0.3s. \end{cases}$$

Fig. 5a presents the voltage regulation through a network of three parallel inverters with heterogeneous DC sources under - 1) change in reference voltage, V_{ref} , 2) change in power sharing requirements, and 3) change in AC-load. Note that Fig. 5a is remarkably identical to Fig. 4 for a single-inverter system, and thus substantiates the equivalence described in Theorem 1. Fig. 5b shows the scaled values of inverter currents $(i_{L_1}/\gamma_1 : i_{L_2}/\gamma_2 : i_{L_3}/\gamma_3)$. As can be seen from the figure, the resultant scaled currents overlap with each other, thereby establishing that the power gets divided in the ratio $\gamma_1 : \gamma_2 : \gamma_3$. Note that the proposed controller provides for faster sharing than the droop-based methods, and even more so with very small voltage tracking error.

VI. CONCLUSIONS AND FURTHER WORK

In this paper, we propose a scalable power sharing architecture for a network of parallel voltage source inverters (VSIs) to overcome the limitations of the droop-based control strategies, while still retaining the advantages of droop based designs. In particular, the proposed design achieves multiple performance objectives simultaneously- (a) Output voltage and frequency regulation at the PCC in presence of *unknown* and *time-varying* loads, (b) Scalability by allowing interfacing of multiple VSIs, (c) Stability and performance

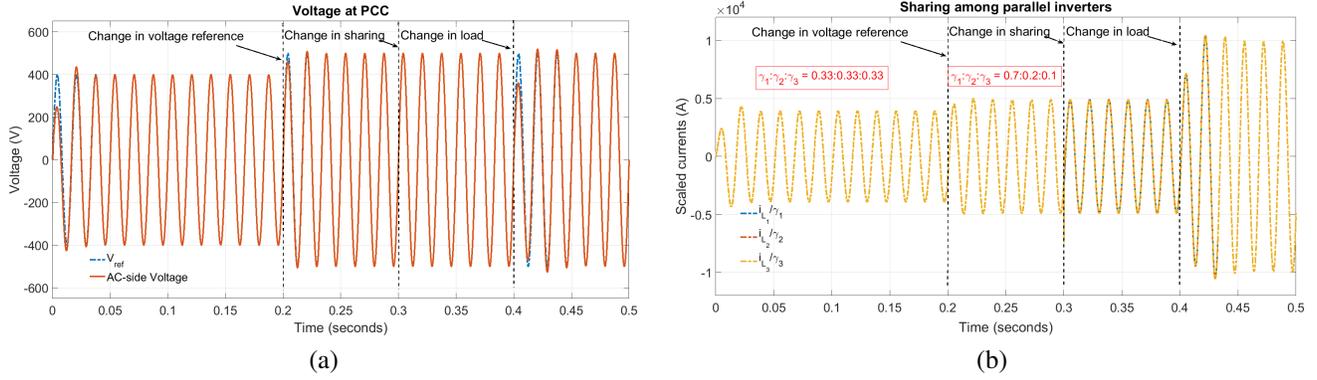


Fig. 5: Results for a network of three parallel inverters for (a) Voltage regulation (b) Power sharing.

analysis of the multi-inverter system, (d) Power sharing, (e) Robustness to model parameters, and (f) Enabling choice of low-order controllers. The setup to demonstrate the proposed control architecture is under preparation and the experimental results will be reported soon in our subsequent work.

APPENDIX

Proof of Theorem 1: System Equivalence

Proof: Let \tilde{G}_c denote the inner-shaped plant in Eq. (8). For the single inverter system described in Fig. 2c, the AC-side voltage at the PCC is given by

$$V = \underbrace{\left(\frac{G_v \tilde{G}_c K_v}{1 + G_v \tilde{G}_c K_v} \right)}_{:=T} (V_{\text{ref}} - n) - G_v \underbrace{\left(\frac{1}{1 + G_v \tilde{G}_c K_v} \right)}_{:=S} i_{\text{load}}. \quad (10)$$

Thus the tracking error ($V_{\text{ref}} - V$) is given by

$$V_{\text{ref}} - V = S V_{\text{ref}} + T n - G_v S i_{\text{load}} \quad (11)$$

For the parallel inverter system in Fig. 3, the AC-side voltage V is given by

$$V = G_v \left(-i_{\text{load}} + \sum_{k=1}^m \gamma_k \tilde{G}_c K_v (V_{\text{ref}} - V - n_k) \right). \quad (12)$$

Using the fact that $\sum_{k=1}^m \gamma_k = 1$ and $\sum_{k=1}^m \gamma_k n_k = n$, and from Eq. (12) one obtains

$$V = T (V_{\text{ref}} - n) - G_v S i_{\text{load}}, \quad (13)$$

which is identical to Eq. (10) and thus yields identical expression for $V_{\text{ref}} - V$. Similarly, the inductor current i_L in Fig. 2c is given by

$$i_L = \tilde{G}_c K_v (V_{\text{ref}} - V - n). \quad (14)$$

The inductor current in the k^{th} inverter in Fig. 3 is given by $i_{L_k} = \gamma_k \tilde{G}_c K_v (V_{\text{ref}} - V - n_k)$. Summing it over k yields

$$\sum_{k=1}^m i_{L_k} = \tilde{G}_c K_v (V_{\text{ref}} - V - n) = i_L, \quad (15)$$

which establishes the required equivalence. ■

Proof of Theorem 1: Power Sharing

Proof: The power sharing scheme follows directly from the construction. Note that the inductor current $i_{L_j} = \gamma_j \tilde{G}_c K_v (V_{\text{ref}} - V - n_j)$. Therefore for inverters j and k , we have

$$\frac{i_{L_j}}{\gamma_j} - \frac{i_{L_k}}{\gamma_k} = \tilde{G}_c K_v (n_k - n_j). \quad (16)$$

Since the measurement-noises are bounded, i.e., $|n_k(j\omega)| \leq \epsilon(\omega) \forall k \in \{1, \dots, m\}$, from (16) we conclude that

$$\left| \frac{i_{L_j}(j\omega)}{\gamma_j} - \frac{i_{L_k}(j\omega)}{\gamma_k} \right| \leq |\tilde{G}_c(j\omega)| |K_v(j\omega)| \epsilon(\omega). \quad (17)$$

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